High Isolation and Low Insertion Loss Switch IC Using GaAs MESFET's

Yorito Ota, Makoto Sakakura, Kazuhisa Fujimoto, Shinji Yamamoto, and Hiromasa Fujimoto

***Abstract*—A novel RF switch IC using GaAs MESFET's has been developed for digital communication systems. The new IC is composed of a three-stage SPST switch and a thin film termination resistor, which realizes a high isolation and a low return loss. In addition, a high power handling capability and a low insertion loss are simultaneously realized with two kinds of pinch-off voltages using the orientation effect of GaAs MESFET's. According to these technologies, the excellent performance is achieved as follows: the isolation of 60 dB, the return loss of 20 dB, the 1 dB power compression of 27 dBm and the insertion loss of 1.6 dB at a frequency of 1.9 GHz with control voltages of 0/−5 V. The new switch IC contributes to a variety of communication system using high-quality digital modulation.**

I. Introduction

RF switch technologies using GaAs MESFET's have advanced as solid state T/R modules for phased array radars in X-band to K/Ka-band [1], [2]. Recent popularization of mobile telecommunication systems has accelerated the GaAs switch technologies in L-band. Low insertion loss SPDT switches are applied to digital personal communication systems such as PHS (Personal Handy-Phone System; in Japan) and DECT (Digital European Cordless Telephone), because their high speed and low power consumption characteristics are suitable for the systems [3], [4]. On the other hand, a high isolation property of a RF switch is required for a base station unit using TDMA (Time Division Multiple Access) communication and for a frequency synthesizer system. The high isolation switch reported [5] was a hybrid IC module composed of shielded microstrip lines and dual-gate GaAs MESFET's. In order to apply these switch IC's to various communication systems, the reduction of size and weight is one of the most important factors. We have introduced a one-chip high-isolation IC in order to reduce them drastically.

The newly-developed switch IC using GaAs MESFET's is fabricated with a novel structure and a simple process. Figs. 1 and 2 show a schematic circuit diagram and a top view photograph of the switch IC. The features of the switch IC are as follows: 1) three-stage SPST switch is integrated on one chip in order to achieve high isolation, 2) the gate orientation effect is introduced to the FET arrangement in order to realize two kinds of pinch-off voltages and consequently obtain high power handling capability and low insertion loss, 3) a 50 Ω termination composed of a shunt-FET and a thin film resistor is employed in order to improve return loss.

In this paper, the fabrication process and the device design of GaAs MESFET's suitable for the switch IC are first presented. The circuit design for isolation, return loss, insertion loss and power handling capability is investigated through the evaluations of single-stage SPST switch IC's and a package. Then, the characteristics of the new switch IC are described.

Manuscript received January 20, 1995; revised May 25, 1995.

Y. Ota and K. Fujimoto are with the Semiconductor Research Center, Matsushita Electric Industrial Co., Ltd., Moriguchi, Osaka 570, Japan.

M. Sakaura is with the Materials and Devices Laboratory, Matsushita Electric Industrial Co., Ltd., Moriguchi, Osaka 570, Japan.

IEEE Log Number 9413432.

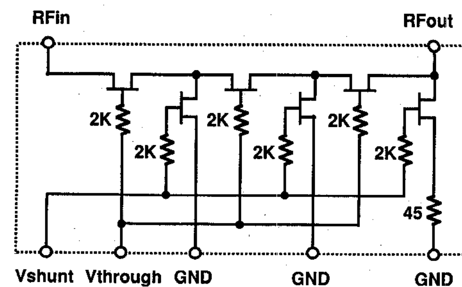

Fig. 1. Circuit diagram of the developed three-stage switch IC.

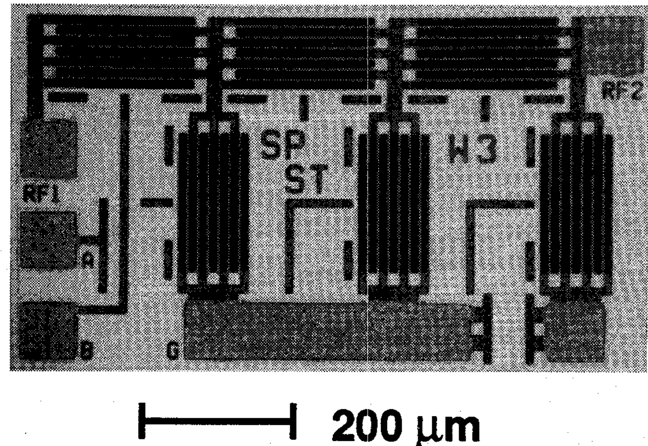

Fig. 2. Photograph of the three-stage switch IC; the through-FET toward [0-1-1] and the shunt-FET toward [0-11] on a (100) GaAs substrate.

II. Fabrication Process and Device Design

GaAs MESFET's in the switch IC's were fabricated by ion-implantation and recess etching process with Al gate metal [6]. The process introduces shallow ion-implantation (acceleration energy of Si^+ = 80 KeV) and shallow recess etching (recess depth <30 nm), while the conventional process employs deep ion-implantation (>100 KeV) and deep recess etching (>100 nm). The channel region with this shallow process exhibits a steeper carrier profile, a higher current density and a shallower pinch-off voltage. These features are suitable for low-voltage operated switch IC's. All FET's in this study have the same device dimensions as follows: the gate length of 1 μm, the finger length of 200 μm and the gate width of 1.2 mm. The gate-to-drain and the gate-to-source distances were minimized up to 0.5 μm in order to reduce a turn-on resistance and consequently reduce insertion loss.

The 2 KΩ gate resistors in Fig. 1 and n^+ contact regions for drain and source in the MESFET's were simultaneously formed by a single ion-implantation (Si^+ = 150 KeV) in order to decrease processing steps. A 50 Ω termination whose value directly influences the return loss property in switch IC's needs to be formed precisely. We fabricated it with a shunt-FET and a thin film NiCr resistor, because the value deviation of the NiCr resistor was less than 5% while that of the ion-implantation resistor was around 20%. Since the turn-on resistance of the shunt-FET was evaluated to be 5 Ω, the thin film resistor was set to 45 Ω for the 50 Ω termination.

The wiring on the switch IC was formed with a thick metal of 2 μm using a gold-plating technique. The wiring was minimized in

0018–9480/95$04.00 © 1995 IEEE

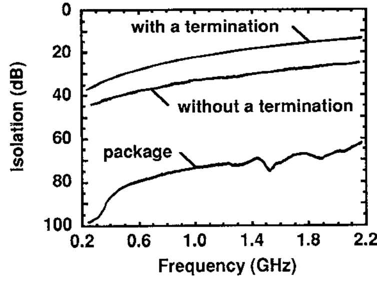

Fig. 3. Isolation of single-stage SPST switches with and without 50 Ω termination, and a package.

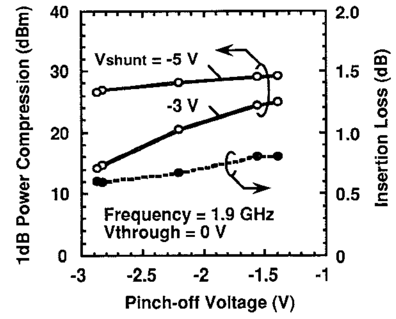

Fig. 4. RF properties dependence on pinch-off voltages of single-stage SPST switches.

order to reduce wiring loss and chip size, as shown in Fig. 2. The total chip size of the switch IC was 0.6 mm × 0.9 mm.

III. Circuit Design and Results

A serial connection of three SPST switches was introduced through the evaluation of a package and a fundamental switch circuit. The isolation property is strongly influenced by a package. We adopted a ceramic package for all RF evaluations. A base metal of the package, on which the switch IC was mounted, was made of gold-plated capper. The base metal was directly soldered on a printed board and was used for a ground plane and a heat sink in order to assure a good ground for RF signal.

To investigate the fundamental circuit properties, we fabricated two types of single-stage SPST switches, with the 50 Ω termination and without it. Fig. 3 shows the experimental results of the isolation of these single-stage switches and the package. All MESFET's in the switches have the same pinch-off voltage of −2.3 V. The bias voltages for the through-FET and the shunt-FET were −5 V and 0 V, respectively. The isolations with the termination and without it were 17 dB and 29 dB at 1.9 GHz, respectively. It was found that the impedance matching using the 50 Ω termination caused the degradation of the isolation property. On the other hand, the return loss was improved from 0.3 dB to 20 dB at 1.9 GHz owing to the termination. The package had a good isolation of −72 dB at 1.9 GHz. In order to make the best use of the package isolation, a three-stage SPST switch with the termination only at the last stages are desirable.

The power handling capability of a through-FET is defined by an allowable voltage swing in the gate. Gopinath and Rankin [7] showed the maximum power handling level of an open-gate through-FET, P_{through}, as follows

$$P_{\text{through}} = I_{dss}|V_p|/4 \tag{1}$$

where I_{dss} and V_p are the saturation current and the pinch off voltage respectively in the through-FET. A large saturation current and a deep pinch-off voltage are required to improve the capability. In case of a shunt-FET, the power handling capability is estimated by an allowable voltage swing in the drain. The maximum power level P_{shunt} protected by a biased shunt-FET is then expressed as follows

$$P_{\text{shunt}} = |V_{gg} - V_p|^2/4Z_0 \tag{2}$$

where V_{gg} ($<V_p$) is a bias voltage, Z_0 is a characteristic impedance of the line connected to the drain. Note that both V_{gg} and V_p are negative. As a matter of course, a large value of P_{shunt} achieves a high power handling capability. Accordingly a shallow pinch-off voltage, which is opposite to the through-FET case, realizes a high capability under the same bias condition.

We prepared single-stage SPST switches which have several kinds of pinch-off voltage for an experimental inspection of the equations. The through-FET and the shunt-FET in each switch have the same pinch-off voltage. Fig. 4 shows the results of the 1 dB power compression level $P_{1\text{dB}}$ and the insertion loss dependences on the pinch-off voltages for the ON-state single-stage switches. The gate bias for the shunt-FET (V_{shunt}) was supplied at −3 V and −5 V, while that for the through-FET (V_{through}) was 0 V. In Fig. 4, the 1 dB power compression level increases as the pinch-off voltage goes shallow. Note that the slope of $V_{\text{shunt}} = -3$ V much depends on the pinch-off voltage in comparison with is that of $V_{\text{through}} = -5$ V. Since P_{shunt} in (2) has a dependence on the gate bias V_{gg}, P_{shunt} dominates the power handling capability and consequently influences $P_{1\text{ dB}}$, under those low bias conditions. Fig. 4 also shows that the pinch-off voltage shallower than −2.2 V for the shunt-FET is required to achieve the 1 dB compression level of 20 dBm at −3 V. On the other hand, the insertion loss, on which the through-FET characteristics directly influences, becomes large as the pinch-off voltage goes shallow. A through-FET with a deep pinch-off voltage generally shows a large saturation current and a small turn-on resistance, and consequently shows a small insertion loss. The reduction of the insertion loss is very important, because the loss becomes triple in our three-stage SPST switch. In order to achieve the insertion loss less than 2 dB (corresponds to 0.65 dB/stage) in the total IC, the pinch-off voltage deeper than −2.4 V for the through-FET is required.

Usually, two kinds of pinch-off voltages are formed by two types of ion implantations [5]. However, the approach increases the processing steps. Asbeck *et al.* [8] first described the orientation effect of GaAs MESFET's. The effect is that piezoelectric charges cause a pinch-off voltage variation along the gate direction of FET's on (100) substrates. We applied their work to the new SPST switch IC to obtain different pinch-off voltages using a single ion implantation. On a (100) semi-insulating GaAs substrate, the through-FET was formed toward [0-1-1] direction which realized a deep pinch-off voltage and the shunt-FET was formed toward [0-11] direction which realized a shallow one. Fig. 5 shows I_{ds}–V_{gs} characteristics of the fabricated through-FET and shunt-FET. By the orientation effect, the through-FET has the pinch-off voltage of −2.5 V and the saturation current of 200 mA, while the shunt-FET has −2.0 V and 180 mA. Each FET has a sufficient margin against the pinch-off voltage which is required above.

Fig. 6 shows the isolation, the return loss and the insertion loss of the newly-developed three-stage SPST switch IC. The bias voltages of 0 V and −5 V were alternatively supplied to the through-FET and the shunt-FET in each measurement. The isolation of 60 dB and the insertion loss of 1.6 dB were achieved at 1.9 GHz. The output return loss was 20 dB at 1.9 GHz, which is the same value as of the single-stage SPST switch with a 50 Ω termination. The new IC shows the 1 dB power compression levels of 20 dBm at the bias voltage of −3 V and 27 dBm at −5 V, which well consists with the expected values as mentioned above.

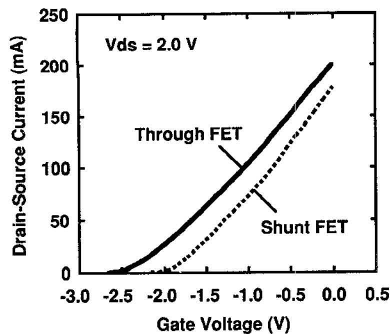

Fig. 5. Comparison of I_{ds}-V_{gs} characteristics between the through FET (solid line) and the shunt FET (dotted line).

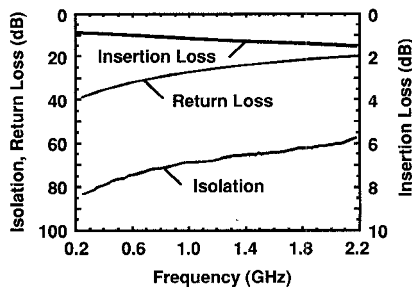

Fig. 6. Small signal properties of the three-stage SPST switch IC.

IV. Conclusion

The approach for high isolation and the improvements for the other RF properties have been investigated. The developed switch IC composed of a three-stage SPST switch and a termination showed good RF characteristics of the isolation of 60 dB and the return loss of 20 dB at 1.9 GHz. The power handling capability and the insertion loss were improved by two kinds of pinch-off voltages using the orientation effect of GaAs MESFET's. The new switch IC contributes to increase various infrastructures for digital communication systems.

Acknowledgment

The authors would like to thank Dr. M. Inada, Dr. O. Ishikawa, H. Kosugi, and K. Nagao for their encouragement. Very special thanks go to Dr. T. Uwano for his valuable suggestions in the preparation of this manuscript.

References

[1] M. J. Schindler and A. Morris, "DC-40 GHz and 20–40 GHz MMIC SPDT switches," *IEEE Trans. Electron Devices,* vol. ED-34, no. 12, pp. 2595–2602, 1987.

[2] D. L. Dunn, P. G. Asher, and C. D. Chang, "Multioctave multithrow active switches," in *IEEE Microwave Theory Tech.-S Dig.,* 1989, pp. 549–551.

[3] S. Kusunoki, T. Ohgihara, M. Wada, and Y. Murakami, "SPDT switch MMIC using E/D-mode GaAs JFET's for personal communication," *IEEE GaAs IC Symp. Dig.,* pp. 135–138, 1992.

[4] H. Uda, T. Sawai, T. Yamada, K. Nogawa, and Yasoo Harada, "High-performance GaAs switch IC's fabricated using MESFET's with two kinds of pinch-off voltages," in *IEEE GaAs IC Symp. Dig.,* 1993, pp. 247–250.

[5] T. Shigematsu, K. Itoh, M. Nakane, and A. Iida, "A shielded microstrip line type high isolation switch," in *Proc. of IEICE FALL Conf.,* Japan 1993, vol. 2, p. 414.

[6] Y. Ota, M. Yanagihara, T. Yokoyama, C. Azuma, M. Maeda, and O. Ishikawa, "Highly efficient, very compact GaAs power module for cellular telephone," in *IEEE Microwave Theory Tech.-S Dig.,* 1992, pp. 1517–1520.

[7] A. Gopinath and J. B. Rankin, "GaAs FET RF switches," *IEEE Trans. Electron Devices,* vol. ED-32, no. 7, pp. 1272–1278, 1985.

[8] P. M. Asbeck, C. P. Lee, and M. F. Chang, "Piezoelectric effects in GaAs FET's and their role in orientation-dependent device characteristics," *IEEE Trans. Electron Devices,* vol. ED-31, pp. 1377–1380, 1984.